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Design Reed Solomon Decoder with Minimum Area Consumption on FPGA

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Abstract: This paper presents a design on Reed Solomon Code for Wi-Max Network. The implementation, written in Very High speed hardware description Language (VHDL) is based on Berlekamp Massey, Forney and Chain Algorithm. The 802.16 network standard recommends the use of Reed-Solomon code RS (255,239), which is implemented and discussed in this paper. It is targeted to be applied in a forward error correction system based on 802.16 network standard to improve the overall performance of the system. The objective of this work is to implement a Reed- Solomon VHDL code to measure the performance of the RS Decoder on Xilinx Spartan 6 (xc6slx100t-3-fgg484) and Xilinx Spartan 3e (xc3s500e-4-fg320) FPGA. The performance of the implemented RS codec on both FPGAs will be compared. The performance metrics to be used are the area occupied by the design and the frequency at which the design can run.

Keywords: Reed Solomon (RS), Galois Field, Generator polynomial, Syndrome calculator, Berlekamp-Massey, Chain search, VHDL, FPGA.

I. INTRODUCTION

Nowadays, we live in a world where communications play an important role both in our daily lives and in their involvement in the economic and technological fields. We constantly need to increase the flow of transmission while maintaining and improving their quality. But without a concern of reliability, all improvement efforts would be futile because it would necessarily mean that some data are to be rebroadcast An error correcting code allows the correcting of one or several errors in a code word by adding redundant symbols to the information, otherwise called, control symbols. Different possible codes exist but in this document we will only deal with Reed Solomon codes because for the moment being, they represent the best compromise between effectiveness (symbols of parity added to the information) and complexity (coding difficulty). Reed-Solomon coding is a very efficient and popular Forward Error Correction technique discovered by Reed and Solomon in 1960[1].Reed-Solomon (RS) codes are among the most widely used block error-correcting codes in digital communication and storage systems [2] and are very Effective in correcting random symbol errors and random burst errors. Therefore they are applied in many systems such as storage devices, mobile communications, and digital Television/DVB, high-speed modems etc. RS codes are adopted by various Standards like DVBT, DVBS, DVB DSNG, DVB C, and IEEE 802.16 WI-MAX.

The purpose of error correction coding can be expressed as increasing the reliability of data communications or data storage over a noisy channel, controlling errors so the reliable reproduction of data can be obtained, increasing the overall system's signal-to-noise energy ratio (SNR), reducing noise effects within a system. The reed-Solomon error correction codes were firstly introduced in the paper "Polynomial codes over certain finite fields" in 1960 for burst error correction.[1].These codes are non-binary systematic cyclic linear block codes. These codes work with symbols that consist of several bits. The mostly used symbol size for non-binary codes is 8-bits, or a byte. A systematic code generates codeword that contain the message symbols in unaltered form. The encoder used mathematical function to the message symbols in order to generate the redundancy, or parity symbols. The basic block diagram for communication system is shown in Figure.1

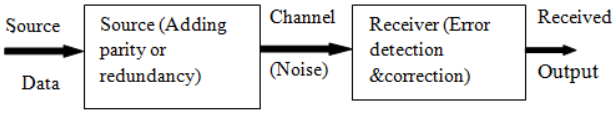

Fig.1 Block diagram of Communication system

A. Types of Error Correcting code

The block and convolution coding are two important classes of error control or channel control coding. Block codes work on fixed-size blocks (packets) of bits or symbols of predetermined size. Practical block codes can generally be decoded in polynomial time to their block length. Convolution codes work on bit or symbol streams of arbitrary. There are many types of block codes, but among the classical ones the most notable is Reed-Solomon coding because of its widespread use on the Compact disc, the DVD, and in hard disk drives. Other examples of block codes include BCH, Hamming, Turbo, Turbo Product, LDPC, fountain codes and BICM codes. The rest of paper is organized as follows. This article is

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structured in six sections. Section II briefly review about Reed Solomon code. Details of the proposed RS Decoder for IEEE 802.16 network are described in Section III. The FPGA implementation and its results are presented in Section IV. Section V provides conclusion

II. REED SOLOMON CODE

RS code is short for Reed-Solomon encoder, which is a kind of non-binary BCH codes, and is particularly applicable in correcting burst errors. Reed Solomon codes have higher error correcting capability that any other codes have. The parameters of RS code are:

m= the number of bits per symbol
n= the block length
k = the uncoded message length in symbols
(n- k) = the parity check symbols (check bytes)
t= the number of correctable symbol errors.

Reed Solomon (RS) codes are a subset of BCH codes and also in a class of linear block codes. A RS code is specified as RS (n, k) with s-bit symbols. This means that the encoder takes k data symbols of s bits each and adds parity symbols to make an n symbol codeword. There are n – k parity symbols of s bit each. A RS decoder can correct up to t symbols that contain errors in a codeword, where 2t = n – k. Figure.1 shows a typical RS codeword which is also known as a systematic code.

DATA	PARITY
k	2t

Fig.2 Typical RS codeword format

III. PROPOSED RS DECODER DESIGN

A. Theory of Reed Solomon decoder

A decoder can correct up to t errors or up to 2t erasures. At decoder, there are three possible conditions when a codeword is decoded a) If 2s+r<2t, (s errors r erasures), then the original transmitted codeword always be recovered. b) The decoder detects that it cannot recover the original codeword and indicates this fact. The decoder misses to decode and recover an incorrect codeword without any indication. The probability of each of these three possibilities depends on the particular RS code chosen, the number of errors and the distribution of errors. The amount of processing "power" required to encode and decode Reed-Solomon codes is related to the number of parity symbols per codeword. A large value of t means that a large number of errors can be corrected but requires more computational power than a small value of t. Table I summarizes RS code specification for 802.16 Wi-Max network standards.

The error correcting ability could be defined as t= (n-k)/2 in RS (n, k), in which n is the length of codeword and k is the length of source data. So a typical system RS codeword is comprised of k symbols source data and n-k symbols redundancy(parity check). RS encoder could be designed by a LFSR, but the decoder is more complex. A common decoder is made of syndrome computation (SC), key equation solver consideration. The Reed-Solomon codes are based on abstract algebra and uses finite Field theory, known as Galois Field. The Galois Fields are implemented according to a primitive polynomial. The primitive polynomial for the RS (255,239), established by the 802.16 standard is given by expression in (1)

Code specification	
Symbol width(Bits / symbol)	s
Field generator polynomial	$P(x)=X^8+X^4+X^3+X^2+1$
Code generator polynomial	$g(x)=(x+\mu^1)(x+\mu^2\ldots)(x+\mu^{21})$
Symbols per block(n)	255
Data symbols per block(k)	239

Table I: RS code specification for 802.16 Wi-Max

$$P(X) = X^8 + X^4 + X^3 + X^2 + 1 \quad (1)$$

The polynomial must be primitive, so that all of its roots are primitive elements, represents as powers of α. It means that all field elements can be represented by using powers of α, ranging from 1 to the number elements of the field minus 1.

The Encoder receives blocks of 239 information bytes and calculates on the 16 parity bytes for each incoming information block. Since the encoder is systematic, the 239 information symbols are transmitted unaltered. To form a 255 bytes codeword the parity bytes are appended at the end of the information block. The Decoder receives the corrupted channel data, detects the error locations, calculates the error magnitudes and corrects the errors. It can detect and correct up to eight errors introduced in the 255 bytes codeword. The decoder marks the codeword as uncorrectable, asserts the corresponding flag and the information is sent out without correction if the encountered errors are greater than 8. Data can be received continuously or with gaps.

B. Design of Reed Solomon decoder

Channel coding systems based on Reed Solomon FEC codes, play a crucial role in today's digital transmission and storage systems. RS decoder is mainly composed of various parts which are calculating syndrome, calculation of error locations and error value polynomial, calculation of error locations and error value and modeling between error patterns and original input vector. Today there are mainly two modes of seeking key equations: Berlekamp-Massey (BM) algorithm and (Euclid) algorithm[8]. DilipV.Sarwate proposed a kind of RiBM algorithm by the very large-scale integrated circuit architecture [3-5] which

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has shorter time delay, more regular architecture and is easy to realize by the VHDL language.

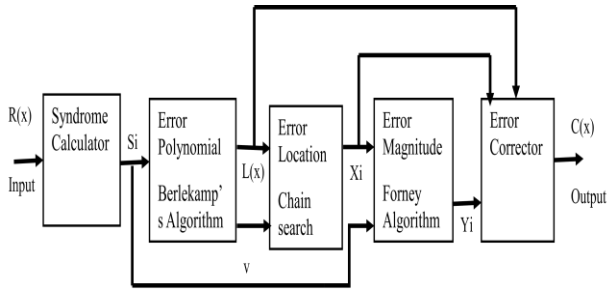

Fig.3 RS decoder Block diagram

The proposed RS decoder model contains the syndrome calculation (SC) block, Error locator block, Chien search and Forney algorithms (CSFA) blocks and Error corrector as shown in Fig. 3

1) Syndrome Calculator

The first step in decoding the received symbol is to determine the data syndrome. Here the input received symbols are divided by the generator polynomial. The result should be zero. The parity is placed in the codeword to ensure that code is exactly divisible by the generator polynomial. If there is a remainder, then there are errors. The remainder is called the syndrome. The syndromes can then be calculated by substituting the 2t roots of the generator polynomial g(x) into R(x). The process is then iterated for other symbols and net 2t syndromes are obtained as soon as the last parity symbol has been read in. The syndromes depend only on the errors, not on the underlying encoded data. [6].

2) BM Algorithm

To find error polynomial, this requires solving 2t simultaneous equation, one for each syndrome. The 2t syndromes form a simultaneous equation with unknowns. The unknowns are the location of errors. The process of solving the simultaneous equation is usually split into two stages. First, an error location polynomial is found. This polynomial has roots which give the error locations. Then the roots of error polynomial are found. The algorithm iteratively solves the error locator polynomial. If it turns out that it cannot solve the equation at some step, then it computes error and weights it, increase the size of error polynomial. A maximum of 2t iterations are required. For n symbols error, the algorithm gives a polynomial with n coefficients. At this point the decoder fails if there are more than t errors, and no corrections can be made [9].

3) Chain search algorithm

Once the error polynomial lambda is known, its roots define where the errors are in the received symbol block. The most commonly used algorithm for this the chain search. All 2^m possible symbols are substituted into the error polynomial, one by one, and the polynomial evaluated. If the result comes to zero, you have a root.

4) Forney algorithm

The next step is to use the syndromes and the error polynomial roots to derive the error values. This is done using the Forney algorithm. This algorithm is an efficient way of performing a matrix inversion. The algorithm works in two stages. First the error evaluator polynomial is calculated. This is done by convoluting the syndromes with error polynomial. If a bit is set in error symbol, then the corresponding bit in the received symbol is in error and must be inverted.The received symbol is XOR with error bit and corrected symbol is obtained.

IV. FPGA IMPLEMENATION OF REED SOLOMON DECODER

Reconfigurable technology is an advance field of study derives from the advantages and applications of FPGA. The flexible hardware can be reconfigured by parameters which determine the architectures of the logic design for different systems according to the resemblance among the algorithms [6]. Hence, a reconfigurable RS Decoder could be designed to reduce the consumption of hardware and complexity.

A. FPGA Implementation Results

The decoder is synthesized targeting Xilinx Spartan 6 FPGA to measure the performance of the implemented RS code, which is compared to the performance of the Reed Solomon code provided by Xilinx Spartan 3e FPGA. The Performance comparison in terms of resource utilization of FPGA and timing performance of the decoder are shown in Table II and Table III, respectively.

Table II Resource utilization of Xilinx Spartan 6 and Spartan 3e FPGA

FPGA Device	Spartan 3e (xc3s500e-4-fg320)	Spartan6 (xc6slx100t-3-fgg484)
Speed Grade	-5	-3
Maximum Frequency	116.19MHz	166.029MHz

Table III Timing performance of Xilinx Spartan 6 and Spartan 3e FPGA

FPGA Device	Spartan 3e (xc3s500e-4-fg320)		Spartan6 (xc6slx100t-3-fgg484)	
Resource Type	Used	Ratio	Used	Ratio
Slice register	1043 out of 9312	11%	144 out of 126576	1%
Slice LUTS	3408 out of 9312	7%	188 out of 63288	2%
IOBS	1 out of 232	1%	23 out of 296	7 %

The simulation waveform Decoder schematic as designed

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using Xilinx 13.1 design tool and is shown in fig.4 and fig 5 respectively.

Fig.4 Simulation Waveform for RS (255,239) Decoder

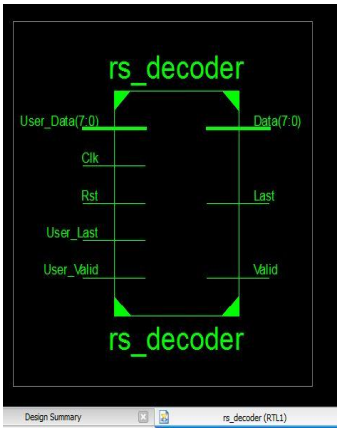

Fig.5 RTL view of RS Decoder showing input and output port

B. Comparison of FPGA architecture

The structural element in an FPGA that is in highest demandfor an FEC application is the Look Up Table (LUT).The VHDL description was implemented in a Xilinx Spartan 6 (xc6slx100t-3-fgg484)FPGA and Spartan 3e (xc3s500e-4-fg320) using the Xilinx ISE version 10.1. Table II and III summarizes the comparison of logic utilization and timing performance. We observe from this comparison table II that Reed Solomon Decoder implemented on Spartan 6 FPGA can save a lot of area. This represents reduction in cost and hardware complexity for the system. Maximum frequency for this case is also found to be higher than that of Spartan 3eimplementation.

V CONCLUSION

In this paper, FPGA implementation of RS Decoder has been presented to analyze performance of wireless communication system particularly for 802.16 network standard. Reed- Solomon (RS) code has been widely used in the FEC systems and provides an excellent way for correcting both random and burst errors. High performance FEC algorithms can be implemented for 802.16 networks using single FPGA devices. This paper demonstrates the implementation RS decoder for Wireless Communication systems, according to the 802.16 standard. The implementation results shows that the designed RS Decoder is capable of efficient correction of errors in wireless applications to provide high performance solution for 802.16 based wireless communication system. The implementation shows an area and complexity reduction in an FPGA.

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BIOGRAPHIES

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